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| 10/699,047      | 10/30/2003  | Ji-young Kim         | 9898-300            | 1200             |

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EXAMINER

DUONG, KHANH B

|          |              |
|----------|--------------|
| ART UNIT | PAPER NUMBER |
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2822

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/699,047

Applicant(s)

KIM, JI-YOUNG

Examiner

Khanh B. Duong

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 01 June 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 8-15 and 17-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 8-15 and 17-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114.

Applicant's submission filed on June 1, 2005 has been entered.

### ***Response to Amendment***

Accordingly, claims 8, 9, 11-14 were amended, and new claims 17-22 were added.

Currently, claims 8-15 and 17-22 are pending.

### ***Allowable Subject Matter***

The indicated allowability of claims 8-15 (currently amended) is withdrawn in view of the newly discovered reference(s) to Lu (US 5,362,665), Ishikawa et al. (US 6,482,701) and Chang et al. (US 6,509,233), and previously cited references to Durcan et al. (US 6,780,732) and Cha (KR 2001-0064328). Rejections based on the newly cited reference(s) follow.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

**Claims 14 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

Claim 14 recites the limitation "the etching time" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

\*\*\* Claim 17 is rejected as depending on claim 14.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**Claims 8, 11, 15 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Lu (US 5,362,665).**

Re claims 8, 11, 15 and 19 Lu discloses in FIGs. 3A-6B a method of forming a MOSFET having a recessed channel, comprising: forming a trench 14 in a semiconductor substrate 8, forming a gate dielectric layer 20 (silicon oxide) on an inner wall and a bottom of said trench 14; sequentially forming a gate conductive layer 22 and a capping layer 24 on the gate dielectric layer 20 so as to fill the trench 14; forming a gate electrode 28 having a first portion which rises over the semiconductor substrate 8 and a second portion filling the trench 14 by patterning the capping layer 24 and the gate conductive layer 22, wherein the first portion has a smaller critical dimension (height) than that of the second portion [see illustration of FIG. 6B below]; forming a source/drain region 30 by implanting impurity ions into the semiconductor substrate 8 on both sides of the gate electrode 28, wherein the source/drain region 30 is shallower than the bottom of the trench 14; forming spacers 32 on the sidewalls of the gate electrode 28.

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

**Claims 9, 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu in view of Ishikawa et al. (US 6,482,701).**

Re claims 9 and 18, Lu discloses forming a rectangular trench 14 in the semiconductor substrate 8 using an anisotropic etch process, but fails to disclose making the trench have a round profile by further etching the trench using a chemical dry etching.

Ishikawa et al. ("Ishikawa") teaches in FIGs. 1A-1D making a trench 5, which was etched using an anisotropic (RIE) etch process, have a round profile by further etching the trench 5 using a chemical dry etching [see col. 3, line 26 to col. 4, line 60].

Since Lu and Ishikawa are from the same field of endeavor, the purpose disclosed by Ishikawa would have been recognized in the pertinent prior art of Lu.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method of Lu as taught by Ishikawa, since Ishikawa states at column 1, lines 35-48 that such modification would reduce not only deterioration in film quality or thinning of a gate oxide, but also electric field at the corner of a bottom portion of the trench. As a result, a withstand voltage breakdown would be minimized at such corner.

Re claim 10, Lu discloses the rectangular trench is formed to a depth of about 0.1 to 0.7 micrometers (1,000 to 7,000 angstroms). Ishikawa discloses the rectangular trench is formed to a depth of about 4 to 6 micrometers (40,000 to 60,000 angstroms) and is further etched to about 0.10 to 0.20 micrometers (1,000 to 2,000 angstroms) using a chemical dry etch process. However, both Lu and Ishikawa fail to disclose the specific ranges of depths as claimed.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize and select appropriate depths for the trench. The selection of

Art Unit: 2822

parameters such as energy, power, concentration, temperature, time, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. “Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce new and unexpected result which is different in kind and not merely degree from results of prior art ... such ranges are termed ‘critical ranges’ and the applicant has the burden of proving such criticality ... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation”. *In re Aller*, 105 USPQ 233, 235 (CCPA 1955). See also MPEP 2144.05.

**Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lu in view of Durcan et al. (US 6,780,732).**

Re claim 12, Lu fails to disclose forming a gate conductive layer comprising a conductive polysilicon layer that fills the trench and a metal layer on the conductive polysilicon layer.

Durcan et al. (“Durcan”) teaches in FIG. 20 forming a gate conductive layer 90 comprising a conductive polysilicon layer 33 that fills the trench 20 and a metal layer 37 on the conductive polysilicon layer 33 [see col. 5, lines 13-54].

Since Lu and Durcan are from the same field of endeavor, the purpose disclosed by Durcan would have been recognized in the pertinent prior art of Lu.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method of Lu as taught by Durcan, since Durcan states at

column 5, lines 23-29 that such modification would form low resistance and low resistivity conductive regions on top of the polysilicon gates 33.

**Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lu in view of Chang et al. (US 6,509,233).**

Re claim 13, Lu fails to disclose forming a sacrificial oxide layer in the trench by thermally oxidizing the semiconductor substrate; and removing the sacrificial oxide layer using a wet etch process.

Chang et al. ("Chang") suggests forming a sacrificial oxide layer in a trench by thermally oxidizing the semiconductor substrate; and removing the sacrificial oxide layer using a wet etch process to remove defects created by a prior etch (RIE) process to form the trench [see col. 3, lines 25-35].

Since Lu and Chang are from the same field of endeavor, the purpose disclosed by Chang would have been recognized in the pertinent prior art of Lu.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method of Lu as suggested by Chang because of the desirability to remove defects created by a prior etch process to form the trench.

**Claims 14, 17, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu in view of Cha (KR 2001-0064328).**

Re claims 20 and 22, see discussions above regarding claims 8 and 19.

Re claims 14, 17 and further claim 20, Lu fails to disclose recessing the gate conductive layer that fills the trench to a depth of 500 Angstroms or less from the surface of the



semiconductor substrate by adjusting an etching time, and forming spacers on the sidewalls of the gate electrode, wherein a portion of the spacers are extended into the semiconductor substrate.

Cha expressly teaches in figs. 1a-1d recessing the gate conductive layer 26 that fills the trench 22 to a certain depth from the surface of the semiconductor substrate 10 by inherently adjusting an etching time, and forming spacers 32 on the sidewalls of the gate electrode 26', wherein a portion of the spacers 32 are extended into the semiconductor substrate 10 [see English Abstract].

Since Lu and Cha are from the same field of endeavor, the purpose disclosed by Cha would have been recognized in the pertinent prior art of Lu.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Lu as taught by Cha for the purposes of insulating the gate electrode and preventing a short channel effect and a hot carrier effect.

Furthermore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize and select an appropriate depth and time for the etching process. The selection of parameters such as energy, power, concentration, temperature, time, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce new and unexpected result which is different in kind and not merely degree from results of prior art ... such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality ... More particularly, where the

general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation”. *In re Aller*, 105 USPQ 233, 235 (CCPA 1955). See also MPEP 2144.05.

**Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lu and Cha as applied to claims 20 and 22 above, and further in view of Ishikawa.**

Re claim 21, Lu discloses the trench is formed to a depth of about 0.1 to 0.7 micrometers (1,000 to 7,000 angstroms), but fails to disclose further etching the trench. Similarly, Cha fails to disclose any further etching of the trench.

Ishikawa teaches in FIGs. 1A-1D a rectangular trench 5 is formed to a depth of about 4 to 6 micrometers (40,000 to 60,000 angstroms) and is further etched to about 0.10 to 0.20 micrometers (1,000 to 2,000 angstroms) using a chemical dry etch process. However, Ishikawa fails to disclose the specific ranges of depths as claimed.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize and select appropriate depths for the trench. The selection of parameters such as energy, power, concentration, temperature, time, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. “Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce new and unexpected result which is different in kind and not merely degree from results of prior art ... such ranges are termed ‘critical ranges’ and the applicant has the burden of proving such criticality ... More particularly, where the general conditions of a claim

Art Unit: 2822

are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In re Aller*, 105 USPQ 233, 235 (CCPA 1955). See also MPEP 2144.05.


### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Weis (US 2002/0196651 A1) disclose in FIG. 2 a MOSFET having a recessed channel, wherein a gate electrode 34 having a first portion which rises over the semiconductor substrate and a second portion filling the trench, wherein the first portion has a smaller critical dimension (width) than that of the second portion.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh B. Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on 10:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
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